What is claimed is:

1. A semiconductor device in which a microprocessor is coupled with a semiconductor memory capable of being accessed by the microprocessor,

wherein the microprocessor comprises an input/output buffer for system side that is made capable of exchanging signals with the outside by being supplied with a power supply voltage,

wherein the semiconductor memory comprises:

an internal power supply circuit that takes in the power supply voltage as a reference voltage, and generates an internal power supply voltage being substantially equal to the power supply voltage; and

an input/output buffer for memory side that is made capable of exchanging signals with the input/output buffer for system side by being supplied with the internal power supply voltage.

2. A semiconductor device according to Claim 1,

wherein the semiconductor memory comprises a dedicated external terminal for taking in the power supply voltage as the reference voltage.

3. A semiconductor device according to Claim 2,

wherein the microprocessor comprises internal circuits

that are put in operation by being supplied with the power supply voltage.

4. A semiconductor device according to Claim 3,

wherein the internal power supply circuit comprises:

a differential circuit that compares the power supply voltage taken in with an output voltage of the internal power supply circuit; and

a voltage output circuit that determines a level of the internal power supply voltage on the basis of a comparison result in the differential circuit.

5. A semiconductor device according to Claim 4,

wherein the semiconductor memory comprises a memory internal circuit that is put in operation by being supplied with a second internal power supply voltage of a higher level than the internal power supply voltage, and

wherein the input/output buffer for memory side comprises a level shifting circuit capable of shifting a signal level of the internal power supply voltage into a signal level of the second internal power supply voltage.

6. A semiconductor device according to Claim 4,

wherein the semiconductor memory comprises:

a step-down circuit that generates a third internal power

supply voltage of a lower level than the internal power supply voltage; and

a memory internal circuit that is put in operation by being supplied with the third internal power supply voltage, and

wherein the input/output buffer for memory side comprises a level shifting circuit capable of shifting a signal level of the third internal power supply voltage into a signal level of the internal power supply voltage.

7. A semiconductor device in which a microprocessor is coupled with a semiconductor memory capable of being accessed by the microprocessor,

wherein the microprocessor comprises:

an internal core power supply circuit that steps down a power supply voltage externally supplied to thereby generate an internal core power supply voltage; and

an input/output buffer for system side that is made capable of exchanging signals with the outside by being supplied with the internal core power supply voltage, and

wherein the semiconductor memory comprises:

an internal power supply circuit that takes in the internal core power supply voltage as a reference voltage, and generates an internal power supply voltage being substantially equal to the internal core power supply voltage; and

an input/output buffer for memory side that is made

capable of exchanging signals with the input/output buffer for system side by being supplied with the internal power supply voltage.

8. A semiconductor device according to Claim 7,

wherein the semiconductor memory comprises a dedicated external terminal for taking in the internal core power supply voltage as the reference voltage.

9. A semiconductor device according to Claim 8,

wherein the microprocessor comprises internal circuits that are put in operation by being supplied with the power supply voltage.

10. A semiconductor device according to Claim 9,

wherein the internal power supply circuit comprises:

a differential circuit that compares the power supply voltage taken in through the external terminal with an output voltage of the internal power supply circuit; and

a voltage output circuit that determines a level of the internal power supply voltage on the basis of a comparison result in the differential circuit.

11. A semiconductor device according to Claim 7,

wherein the microprocessor comprises a clock driver

capable of outputting a clock signal, and

wherein the semiconductor memory comprises:

a clock buffer that takes in the clock signal outputted through the clock driver in the microprocessor; and

a logic circuit that operates synchronously with the clock signal taken in through the clock buffer.

12. A semiconductor device according to any of Claim 1 through Claim 11,

wherein the microprocessor and the semiconductor memory are each formed in separate chips, and these chips are integrally packaged by a resin mold.